Final Review

CSCI 2021: Machine Architecture and Organization

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Role within Curriculum

CSCI 5221 Networks
CSCI 4061 Operating Systems
CSCI 5204 Computer Architecture
CSCI 1902 Structure of Computer Prog.
CSCI 2021 Machine Arch. & Organization
CSCI 5231 Real-Time and Embedded Sys.
CSCI 4203 Computer Architecture
CSCI 3081 Program Design & Development
CSCI 4611 Graphics and Games
CSCI 5161 Compilers

Transition from Abstract to Concrete!
- From: high-level language model
- To: underlying implementation
Computer Architecture & Compiler

A few 8000-level courses

Parallel Architecture
Embedded Processor
Virtual Machine
Advanced Compiler Tech.

CSCI 5204 Computer Architecture
CSCI 5161 Compilers
Final Reviews

$100

$200

$300

$400
Design a digital circuit that determines if a 4-bit binary number is evenly divisible by 3.
Can you design a D-latch using only NAND gates?

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<tr>
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Design a 4-bit comparator.
Design a sequential circuit that has a one-bit input (x) and a one-bit output (z). In this design, a new bit is read from the input stream in every clock cycle.

The output (z) is 1, if and only if the total number of 1's received from the input (x) is divisible by 3 (e.g. 0, 3, 6). In other words, the input sequence \{0, 0, 1, 1, 0, 1, 0, 1\} will result in the following output \{1, 1, 0, 0, 0, 1, 1, 0\}. 
Answer: $100

0000, 0011, 0110, 1001, 1100, 1111
Answer: $200
Answer: $300
(1) \( A = B : A_3 = B_3, A_2 = B_2, A_1 = B_1, A_0 = B_0 \)

\[ x_i = A_iB_i + A_i'B_i' \]

\[ \text{XOR-Invert} = (A_iB_i' + A_i'B_i)' \]
\[ = (A_i' + B_i)(A_i + B_i') \]
\[ = A_i'A_i + A_i'B_i' + A_iB_i + B_iB_i' \]
\[ = A_iB_i + A_i'B_i' \]

Output: \( x_3x_2x_1x_0 \)
(2) \( A > B \)
Output: \( A_3B'_3 + x_3A_2B'_2 + x_3x_2A_1B'_1 + x_3x_2x_1A_0B'0 \)

(3) \( A < B \)
Output: \( A'_3B_3 + x_3A'_2B_2 + x_3x_2A'_1B_1 + x_3x_2x_1A'_0B_0 \)
Design the comparator with multiplexer
One bit comparator
Answer: $400